## NASA TECH BRIEF

# NASA Pasadena Office



NASA Tech Briefs announce new technology derived from the U.S. space program. They are issued to encourage commercial application. Tech Briefs are available on a subscription basis from the National Technical Information Service, Springfield, Virginia 22151. Requests for individual copies or questions relating to the Tech Brief program may be directed to the Technology Utilization Office, NASA, Code KT, Washington, D.C. 20546.

The second of th

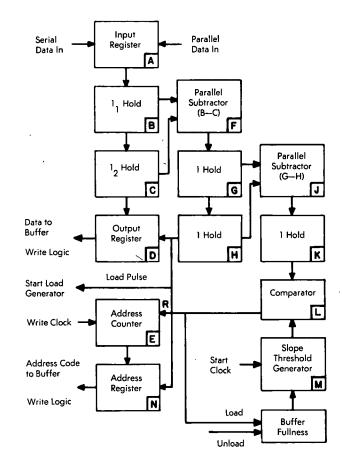
## Digital Slope-Threshold Data Compressor

Video data is compressed before transmission when it is necessary to conserve the bandwidth of a communication channel. The slope-threshold compression scheme for telemetered video data is one of the most efficient, and its principle of operation is as follows: when the slope (first difference) of the raw data exceeds the threshold decision reference, the previous sample is transmitted. The threshold decision reference is a symmetrical bipolar exponential decay function that is biased to the first difference related to the last accepted sample. This scheme has been implemented by analog circuitry; however, analog circuits are frequency dependent, often drift, and require periodic calibration.

The present all-digital design is more economical than an analog system; moreover, it exhibits a welldefined accuracy, provides unlimited storage time with no degradation, and is more convenient and reliable.

The analog design includes two threshold decision reference branches (positive and negative), each biased to the difference sample that related to the last accepted sample. In the all-digital design, the bias is first subtracted from difference samples to be compared. The threshold function can then operate at a common level and the comparison between the difference samples, and the two branches of the exponential decision reference, can be accomplished in a single comparator simply by using the absolute values of both the samples and the reference.

The digital data compression system includes not only the processor, but also a rate buffer and feedback control from the buffer to the processor. The processor shown in the diagram is novel. Continuous



serial or parallel digital data are received in entry register A. Upon word sync, a data word is transferred in parallel to processing register B and at the next word time to processing register C. For one full word time, two consecutive samples are then present in processing registers B and C. A parallel subtractor F is connected between B and C. The difference B—C

(continued overleaf)

is transferred to hold register G. If a sample is accepted, the B—C difference is transferred from G to H and becomes the new bias for the exponential slope threshold decision reference against which all future differences are compared.

To make the comparison simple for both the postive and negative branch of the exponential decision reference, the bias held in H is first subtracted in a parallel subtractor J from all future difference samples in G. A sample in K is then compared in a digital binary comparator to both branches of the decision reference M by using the absolute value of both K and M. For each accepted sample, the run length address from address counter E is transferred to address hold register N for input to the buffer write logic. To simplify the arithmetic implementation, subtraction is accomplished by adding the ones complement of the subtrahend to the minuend. The sign of the output of difference subtractor F indicates the direction of the signal slope.

The magnitude comparator and the ones-complement logic for the first subtractor can be eliminated by adding a digital binary integer bias to the minuend B input so that the difference always will be positive. This positive difference will then also be the minuend G and subtrahend H for the second subtractor J. Since the original bias added to C is contained in both G and H, it is cancelled out in J where the difference G—H is formed. The adder contains eight bits and the input six. Bit seven of the C input to subtractor F is hard-wired to collector voltage  $+V_{cc}$  to form the mentioned bias.

The source sampling rate and the transmission rate are held constant. The data compression system is a redundancy reduction system, and the processor or data compressor tests each sample for significance and retains or rejects samples. It is then necessary to buffer samples that are accepted at a nonuniform rate and transmitted at a uniform rate. The size of the buffer is mainly dependent on the statistics of the signal, but is also dependent on the characteristics of the feedback loop between the buffer and the significance detector. The buffer fullness measure controls the significance criteria. A buffer fullness counter continuously controls the initial starting point of the exponential threshold function and also its time constant. The gain of this feedback can be set for each of those parameters independently to correspond to signal statistics and desired compression ratio. Two other controls in the buffer are included to accept a "confidence" sample if the code length reaches full scale or if the buffer fullness level recedes below a

certain level. The buffer includes input and output registers; if the system is abused and the buffer reaches complete fullness, further load pulses will be inhibited until an unload occurs. Conversely, if the buffer is completely empty, further unload pulses are inhibited until a load pulse occurs. The last unloaded data will remain in the output register for repeated readout.

A feedback control block contains the slope-threshold generator. The buffer fullness measure controls the initial amplitude of the slope-threshold generator and/or its time constant. The value of a decaying exponential function is compared to the value in a digital register, and it is possible to program the initial value and time constant of the exponential function in order to select the desired compression ratio. The method for digital approximation of the exponential function to any desired degree of accuracy uses only simple counters and gating logic. The basic procedure in implementing the quasi-exponential slope generator is to vary the clock rate of a counter in such a manner that the value in the counter is decremented approximately exponentially with time. The initial value in the counter is preset to any desired value, and the time constant is chosen by selection of the basic clock frequency.

### Note:

Requests for further information may be directed to:

Technology Utilization Officer NASA Pasadena Office 4800 Oak Grove Drive Pasadena, California 91103 Reference: TSP 73-10355

#### Patent status:

This invention has been patented by NASA (U.S. Patent No. 3,694,581). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

NASA Patent Counsel Mail Code 1 NASA Pasadena Office 4800 Oak Grove Drive Pasadena, California 91108

> Source: Tage O. Anderson of Caltech/JPL under contract to NASA Pasadena Office (NPO-11630)

B73-10355 Category 02